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10/510,988	10/13/2004	Ryusuke Horibe	60188-962	2223

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EXAMINER	
JONES, CRYSTAL L	

ART UNIT	PAPER NUMBER
2627	

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/510,988	HORIBE ET AL.	
	Examiner	Art Unit	
	Crystal Jones	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-10,13,18,19 and 22* is/are rejected.

7)☒ Claim(s) *3,4,11,12,14-17,20,21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 October 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-5b should be designated by a legend such as --Prior Art—because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 11 is objected to because of the following informalities: "contol" of line 23 should be changed to --control--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 5-10 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by

Shoji et al. (U.S. Publication 2002/0172112).

Regarding claim 1, Shoji et al. disclose a signal processing device for reproducing recorded information on an information recording medium, comprising: a feedback loop including operational amplifier means (Fig. 1, element 2) for amplifying a reproduction signal of the recorded information and a gain/offset control means for controlling a gain (Fig. 1, element 3) and an offset (Fig. 1, element 6) of the operational amplifier means so that each of an amplitude and an offset of an output of the operational amplifier means becomes a predetermined value, respectively ([0086]); and direct-current component extraction means (Fig. 1, element C1) for extracting direct-current component information of the reproduction signal from signals of the feedback loop, wherein the signal processing device supplies the direct-current component information as information indicating an asymmetry amount of the reproduction signal.

Regarding claim 6, Shoji et al. disclose the signal processing device of claim 1, further comprising waveform detection means for detecting, based on the output of the operational amplifier means, information for a waveform of the reproduction signal and supplying the waveform information to the gain/offset control means (Fig. 2, elements 61 and 62).

Regarding claim 7, Shoji et al. disclose the signal processing device of claim 6, wherein the waveform detection means includes: peak detection means for receiving the output of the operational amplifier means as an input and performing peak detection (Fig. 2, element 61); and bottom detection means for receiving the output of the operational amplifier means as an input and performing bottom detection (Fig. 2, element 62).

Regarding claim 8, Shoji et al. disclose the signal processing device of claim 6, wherein the waveform detection means includes: amplitude detection means (Fig. 2, element 63) for receiving the output of the operational amplifier means as an input, detecting an amplitude of the reproduction signal and outputting an amplitude information signal; and offset detection means for receiving the output of the operational amplifier means as an input, detecting an offset of the reproduction signal and outputting an offset information signal ([0100]).

Regarding claim 9, Shoji et al. disclose the signal processing device of claim 6, wherein the waveform detection means includes: peak detection means for receiving the output of the operational amplifier means and performing peak detection (Fig. 2, element 61); bottom detection means for receiving the output of the operational amplifier means and performing bottom detection (Fig. 2, element 62); amplitude detection means for receiving an output of the peak detection means and an output of the bottom detection means as inputs, performing an operation to obtain an output signal amplitude of the operational amplifier means and outputting an amplitude information signal (Fig. 2, element 63); and offset detection means for receiving the output of the peak detection means and the output of the bottom detection means as inputs, performing an operation to obtain an output signal offset of the operational amplifier means and outputting an offset information signal ([100]).

Regarding claim 10, Shoji et al. disclose the signal processing device of claim 1, further comprising equalizer means (Fig. 1, element 4), located between the operational amplifier means and the gain/offset control means, for emphasizing a high frequency band of the output of the operational amplifier means ([0084]).

Regarding claim 22, Shoji et al. disclose a signal processing method for reproducing recorded information on an information recording medium, comprising the steps of: controlling a gain (Fig. 1, element 3) and an offset (Fig. 1, element 6) of an operational amplifier means (Fig. 1, element 2) for amplifying a reproduction signal of the recorded information in a feedback loop so that an amplitude and an offset of an output of the operational amplifier means are set at a predetermined value ([0086]), respectively; extracting a direct-current component (Fig. 1, element C1) information of the reproduction signal from signals of the feedback loop; and supplying the direct-current component information as information indicating an asymmetry amount of the reproduction signal.

4. Claims 1, 5-10 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Horibe (U.S. Publication 2004/0172148).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Horibe discloses a signal processing device for reproducing recorded information on an information recording medium, comprising: a feedback loop including operational amplifier means (Figs. 15, 16, 20 and 22, element 1) for amplifying a reproduction signal of the recorded information and a gain/offset control means (Figs. 15, 16 and 22, elements 8 and 9) for controlling a gain and an offset of the

operational amplifier means so that each of an amplitude and an offset of an output of the operational amplifier means becomes a predetermined value, respectively; and direct-current component extraction means (Fig. 20, element 101) for extracting direct-current component information of the reproduction signal from signals of the feedback loop, wherein the signal processing device supplies the direct-current component information as information indicating an asymmetry amount of the reproduction signal ([0009] lines 8-13).

Regarding claim 5, Horibe discloses the signal processing device of claim 1, wherein when an input reproduction signal of the operational amplifier means is a signal from which a direct-current component has been removed beforehand, offset control information from the gain/offset control means to the operational amplifier means is supplied as information indicating the asymmetry amount (See Fig. 20; DC component is removed beforehand by element 101).

Regarding claim 6, Horibe discloses the signal processing device of claim 1, further comprising waveform detection means for detecting, based on the output of the operational amplifier means, information for a waveform of the reproduction signal supplying the waveform information to the gain/offset control means (Figs. 15, 16, 20 and 22, elements 4 and 5).

Regarding claim 7, Horibe discloses the signal processing device of claim 6, wherein the waveform detection means includes: peak detection means for receiving the output of the operational amplifier means as an input and performing peak detection (Figs. 15, 16, 20 and 22, element 4); and bottom detection means for

receiving the output of the operational amplifier means as an input and performing bottom detection (Figs. 15, 16, 20 and 22, element 5).

Regarding claim 8, Horibe discloses the signal processing device of claim 6, wherein the waveform detection means includes: amplitude detection means for receiving the output of the operational amplifier means as an input, detecting an amplitude of the reproduction signal and outputting an amplitude information signal (Figs. 15, 16, 20 and 22, element 6); and offset detection means for receiving the output of the operational amplifier means as an input, detecting an offset of the reproduction signal and outputting an offset information signal (Figs. 15, 16 and 22, element 7).

Regarding claim 9, Horibe discloses the signal processing device of claim 6, wherein the waveform detection means includes: peak detection means for receiving the output of the operational amplifier means and performing peak detection (Figs. 15, 16, 20 and 22, element 4); bottom detection means for receiving the output of the operational amplifier means and performing bottom detection (Figs. 15, 16, 20 and 22, element 5); amplitude detection means for receiving an output of the peak detection means and an output of the bottom detection means as inputs, performing an operation to obtain an output signal amplitude of the operational amplifier means and outputting an amplitude information signal (Figs. 15, 16, 20 and 22, element 6); and offset detection means for receiving the output of the peak detection means and the output of the bottom detection means as inputs, performing an operation to obtain an output signal offset of the operational amplifier means and outputting an offset information signal (Figs. 15, 16 and 22, element 7).

Regarding claim 10, Horibe discloses the signal processing device of claim 1, further comprising equalizer means, located between the operational amplifier means and the gain/offset control means, for emphasizing a high frequency band of the output of the operational amplifier means (Figs. 15 and 16, element 26).

Regarding claim 22, Horibe discloses a signal processing method for reproducing recorded information on an information recording medium, comprising the steps of: controlling a gain and an offset of an operational amplifier means (Figs. 20 and 22, element 1) for amplifying a reproduction signal of the recorded information in a feedback loop so that an amplitude and an offset of an output of the operational amplifier means are set at a predetermined value, respectively (Fig. 22, elements 8 and 9); extracting a direct-current component information of the reproduction signal from signals of the feedback loop (Fig. 20, element 101); and supplying the direct-current component information as information indicating an asymmetry amount of the reproduction signal ([0009] lines 8-13).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shoji et al. (U.S. Publication 2002/0172112) in view of Noda et al. (U.S. Publication 2004/0257956).

Regarding claim 2, Shoji et al. disclose the signal processing device of claim 1, but fails to disclose the direct-current component extraction means as binarization means.

Noda et al. disclose binarization means ([0027] lines 1-5) for receiving the output of the operational amplifier means as an input and performing binarization while adjusting a slice level by feedback control so that a duty ratio after the binarization becomes a predetermined value (duty cycle can be defined by the ratio of "1's" to "0's" of decoded data "(g)" of Fig. 11.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the signal processing device of Shoji et al. to include the binarization means of Noda et al.

The motivation for such combination is to reconstruct digital data from an analog signal (Noda et al. [0027] lines 1 and 2).

Regarding claim 18, Noda et al. disclose the signal processing device of claim2, as noted in the obvious combination above, further comprising an AD conversion means (Fig. 1, element 107), for sampling the output of the operational amplifier means and then performing analog-to-digital conversion to the output of the operational amplifier means, wherein the binarization means receives sampling data provided by the AD conversion means as an input.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the signal processing device of Shoji et al. to include the AD conversion means located after the operational amplifier means of Noda et al.

The motivation for such combination is to reconstruct digital data from an analog signal.

Regarding claim 19, Noda et al disclose the signal processing device of claim 18, as noted in the obvious combination above, further comprising: Viterbi decoding means (Fig. 1, element 109) for outputting decoded data corresponding to a state transition maximum-likelihood-estimated by Viterbi decoding of the sampling data ([0048] lines 1-4); and judgment level control means for controlling ([0048] lines 6-10), based on the asymmetry amount information, a judgment level of the Viterbi decoding means so that a reproduction error rate is reduced ([0048] lines 6-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the signal processing device of Shoji et al. to include the Viterbi decoding means of Noda et al.

Motivation for such combination is to have a means for decoding digital data while eliminating interference between data (Noda et al. [0037] lines 4-9).

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shoji et al. (U.S. Publication 2002/0172112) in view of Mita et al. (U.S. Patent 5,412,632).

Regarding claim 13, Shoji et al. disclose the signal processing device of claim 1, but fails to disclose defect detection means.

Mita et al. disclose defect detection means for detecting a defect of the reproduction signal (Fig. 1, elements L and M); and holding means (Fig. 1, element 15) for holding (Fig. 1, element 15) the direct-current component information (Fig. 1, information produced from HPF, element 9) during a defect detection period.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the signal processing device of Shoji et al. to include defect detection means.

Motivation for such combination is to overcome defects found in a VFO part (Mita et al., Col. 3, lines 29-45).

7. Claims 2, 18 and 19 are rejected under 35 U.S.C. 103(a) as being obvious over Horibe (U.S. Publication 2004/0172148) in view of Noda et al. (U.S. Publication 2004/0257956).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claim 2, Horibe discloses the signal processing device of claim 1, but fails to disclose the direct-current component extraction means as binarization means.

Noda et al. disclose binarization means ([0027] lines 1-5) for receiving the output of the operational amplifier means as an input and performing binarization while

adjusting a slice level by feedback control so that a duty ratio after the binarization becomes a predetermined value (duty cycle can be defined by the ratio of "1's" to "0's" of decoded data "(g)" of Fig. 11.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the signal processing device of Horibe to include the binarization means of Noda et al.

The motivation for such combination is to reconstruct digital data from an analog signal (Noda et al. [0027] lines 1 and 2).

Regarding claim 18, Noda et al. disclose the signal processing device of claim2, as noted in the obvious combination above, further comprising an AD conversion means (Fig. 1, element 107), for sampling the output of the operational amplifier means and then performing analog-to-digital conversion to the output of the operational amplifier means, wherein the binarization means receives sampling data provided by the AD conversion means as an input.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the signal processing device of Horibe to include the AD conversion means located after the operational amplifier means of Noda et al.

The motivation for such combination is to reconstruct digital data from an analog signal.

Regarding claim 19, Noda et al disclose the signal processing device of claim 18, as noted in the obvious combination above, further comprising: Viterbi decoding means (Fig. 1, element 109) for outputting decoded data corresponding to a state transition maximum-likelihood-estimated by Viterbi decoding of the sampling data ([0048] lines

1-4); and judgment level control means for controlling ([0048] lines 6-10), based on the asymmetry amount information, a judgment level of the Viterbi decoding means so that a reproduction error rate is reduced ([0048] lines 6-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the signal processing device of Horibe to include the Viterbi decoding means of Noda et al.

Motivation for such combination is to have a means for decoding digital data while eliminating interference between data (Noda et al. [0037] lines 4-9).

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being obvious over Horibe (U.S. Publication 2004/0172148) in view of Mita et al. (U.S. Patent 5,412,632).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing

that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claim 13, Horibe discloses the signal processing device of claim 1, but fails to disclose defect detection means.

Mita et al. disclose defect detection means for detecting a defect of the reproduction signal (Fig. 1, elements L and M); and holding means (Fig. 1, element 15) for holding (Fig. 1, element 15) the direct-current component information (Fig. 1, information produced from HPF, element 9) during a defect detection period.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the signal processing device of Horibe to include defect detection means.

Motivation for such combination is to overcome defects found in a VFO part (Mita et al., Col. 3, lines 29-45).

Allowable Subject Matter

9. Claims 3, 4, 11, 12, 14-17, 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 3, no reference alone or in combination discloses direct-current component extraction means as a low pass filter.

Regarding claim 11, no reference alone or in combination discloses adjusting an emphasis amount of the high frequency band of an equalizer means.

Regarding claim 14, no reference alone or in combination discloses smoothing means for smoothing a slice level of a binarization means.

Regarding claim 17, no reference alone or in combination discloses adjusting a binary slice level by applying an offset.

Regarding claim 20, no reference alone or in combination discloses selectively outputting the output of a binarization means or an output of a Viterbi decoding means.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tonami (U.S. Publication 2002/0012308) and Hayami et al. (U.S. Publication 2002/0012306).

Tonami discloses a signal processing device comprising: a DC blocking circuit, automatic gain control, and a decoding circuit but fails to disclose the components configured as claimed.

Hayami et al. disclose a signal processing device comprising: a DC blocking circuit, automatic gain control, and a Viterbi decoder but fail to disclose the components configured as claimed.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Crystal Jones whose telephone number is 571-272-2849. The examiner can normally be reached on Monday through Friday, 8:30 a.m. to 6 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on 571-272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CJ

WAYNE YOUNG
SUPERVISORY PATENT EXAMINER